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PTO/SB/05 (1/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-21570
First Inventor or Application Identifier	Havemann
Title	Enhancements To Polysilicon Gate
Express Mail Label No.	EL162527038US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 14] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages 1]
   - a. [X] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [X] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [XX] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [ ] Other: ....

* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ______/______

Prior application information: Examiner ______ Group / Art Unit: ______

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

Name	Jacqueline J. Garner				
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Name (Print/Type)	Jacqueline J. Garner	Registration No. (Attorney/Agent)	36,144
Signature	[signature]	Date	12/18/98

EXPRESS MAIL Mailing Label Number EL162527638US . I hereby certify th the accompanying application is being deposited with the United States Postal Serv "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indi below and is addressed to the Ass't Commissioner of Patents, Washington, DC 20231.

By: Date:

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 954.

Complete if Known	
Application Number	
Filing Date	12/18/98
First Named Inventor	Havemann
Examiner Name	
Group / Art Unit	
Attorney Docket No.	TI-21570

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [ ] Payment Enclosed: [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	9	-20** =	—	X	22	=	-0-
Independent Claims	5	-3** =	2	X	82	=	164
Multiple Dependent					270	=	-0-

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 164.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) ______

Other fee (specify) ______

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) -0-

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Jacqueline J. Garner	Reg. Number	36,144
Signature	[signature] Date 12/18/98	Deposit Account User ID	---

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Docket No.: TI-21570

Robert H. Havemann Examiner: Not Determined

Serial No.: Not Determined Art Unit: Not Determined

Filed: Herewith

For: Enhancements to Polysilicon Gate

PRELIMINARY AMENDMENT

Assist. Commissioner for Patents
Washington, DC 20231

Dear Sir:

"EXPRESS MAILING" Mailing Label No.
EL162527038US, Date of Deposit: 12-18-98.

Please amend the specification by inserting before the first line the sentence:

This application claims priority under 35 USC § 119 (e) (1) of provisional application number 60/068,962, filed 12/30/97.

Respectfully submitted,

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Enhancements to Polysilicon Gate

Background and Summary of the Invention

The present invention relates to integrated circuit structures and fabrication methods, especially to silicided polysilicon gates.

Background: Gate Resistance

Even as the size of integrated circuits shrinks, the demand for higher performance, including decreased resistance on conductive lines, increases. In logic integrated circuits, polysilicon gate lines commonly use a self-aligned metal silicide, such as titanium silicide, to reduce gate resistance and gate propagation delay. As device sizes shrink, smaller gate sizes mean that there are fewer nucleation centers for the transformation of titanium disilicide from a high resistance state (C49) to a low resistance state (C54), giving less desirable results. Further background in silicided gate structures can be found in Silicon Processing for the VLSI Era, Wolf *et al.*, 1986 (see especially Volume 1, Chapter 11 on "Refractory Metals and Their Silicides in VLSI Fabrication" and Volume 2, Chapter 3 on "Contact Technology and Local Interconnects for VLSI"), which is hereby incorporated by reference.

U.S. Patent 5,196,360 (Doan *et al.*) shows a previous method of forming a silicide on a gate structure. This patent discloses a polysilicon gate with dielectric sidewalls which "extend vertically upward from the source an [sic] drain regions ... to somewhat below the uppermost surface of the gate electrode region". Although this will

leave a small portion of the gate sidewall exposed for silicidation, the process shown uses sputter deposition (PVD) to deposit the metal layer which will be converted into a silicide. Since sputter deposition gives very poor step coverage, this method would not give effective silicide coverage on the sidewalls of the gate. Furthermore, this patent appears to view silicide growth on the sidewalls of the gate as a problem which must be dealt with, rather than a desirable effect.

A commonly owned application (provisional 60/045,178, filed 04/30/97) describes a process in which the height of the sidewall spacers is reduced, so that metal can be deposited along a significant height of the sidewalls for the gate, as well as on top of the gates. In the prior application, this is suggested as a way of reducing the total resistance of a gate line, by in effect reducing the average resistivity of the material, and by changing the overall line-to-phase ratio of the gate pattern, but this prior application still uses gate sidewalls to provide separation between the silicide layer on the gate structure and the silicide on the conductive part of the source/drain regions.

Background: Drain Profile Engineering

One of the long-standing problems in small field effect transistors is hot carrier effects. When a conventional MOS transistor structure is scaled down to one micron or less, the potential energy of an electron changes dramatically when it hits the N+ drain boundaries. This sudden change in potential energy in a short distance creates a high electric field. This is undesirable because it causes the electrons to behave differently within the semiconductor lattice. Electrons which have been activated by high electric fields are referred to as "hot

electrons", and can, for example, penetrate into or through the gate dielectric. Electrons which penetrate into, but not through, the gate dielectric can cause the gate dielectrics to become charged up over time. Thus, the behavior of the transistor will gradually shift in the field, until the transistor may fail in service. This is extremely undesirable. Holes are also subject to the effects of a high electric field, although this is usually not quite as great a concern with holes, due to their higher effective mass in silicon.

To avoid hot carrier effects, several techniques have been proposed. One of these techniques is lightly doped drain extension regions, or "LDD" regions. In this structure, which is now used in most small-dimension transistors, a first light and shallow implant is performed before sidewall spacers are formed on the gate structure. After the sidewall spacers are in place, a second heavier implant is performed. The first implant provides only a relatively low conductivity in the silicon, so that the voltage has a significant gradient across the LDD region. This prevents the voltage difference, between channel and drain, from appearing entirely at the drain boundary. By increasing the distance over which this voltage difference occurs, the peak electric field is reduced, and this tends to reduce channel hot carrier (CHC) effects. Another conventional technique which has been used is the "double doped drain." In this technique, the drain is implanted with both phosphorus and arsenic (or alternatively with both phosphorus and antimony.) Phosphorus diffuses faster, at a given temperature, than arsenic, and thus produces a slightly "fuzzy" drain profile. Again, this has the effect of stretching the voltage change at the drain boundaries, and this reduces the peak electric field, as is

desirable.

Another common technique, which is not done primarily for reasons of drain profiling, but which has some influence on this, is the "smiling" oxidation. After a gate structure has been formed, a further oxidation is commonly performed, to widen the oxide thickness at the lower corners of the gate. This has the effect of slightly increasing the separation between the lower corners of the gate and the silicon substrate. This is desirable, since the electric field is slightly higher at the gate corners, due to geometric effects. This is usually done, however, primarily to compensate for any damage to the gate dielectric at the lower gate corners which may be caused by etching processes.

Enhancements to Gate Conductivity and Drain Profile Engineering

The present application provides several innovations which are aimed at optimizing the conductivity of gate structures, and also provide new tools for drain profiles engineering.

Preferably, in one embodiment of the disclosed method, an oxidation resistant sidewall layer is applied to the gate structure, to permit a "smiling" oxidation be performed to elevate the corners of the gate structure. The sidewalls of the gate are then exposed and a metal for siliciding is deposited overall, after which source/drain implants are performed. Optionally, additional source/drain implants can be performed prior to metal deposition. After an implant has been done through the metal, an annealing step is applied, to cause silicidation, and also to activate the implant into the source/drain regions. The unreacted metal is then stripped, providing a polysilicon gate which is heavily coated with silicide. If desired, additional dielectric sidewall

layers can be added onto the silicide sidewalls after the metal is stripped, to assure a safe offset between the silicide and the drain siliciding. If desired, the source/drains can be silicided separately from the gates, to provide, e.g., two different silicide compositions on the source/drains and on the gates.

Preferably, in another embodiment of the disclosed method, after a smiling oxidation is performed and the nitride sidewalls removed, the sidewalls of the gate structure are extended by a conformal polysilicon deposition. Thus, the location of the smiling oxidation does not have to be aligned to the corners of the gate, as has conventionally been desired. This opens up a new range of options in drain profile engineering. The gate-induced electric field can be removed from the drain region, by an amount which is independent of the separation between N+ and N- (or alternatively P+ and P-) diffusions.

Advantages of the disclosed methods and structures include:

- increased gate conductivity;
- additional control over gate corner profiles;
- additional control over gate electric fields;
- additional control over silicided gate structures;
- additional control over the line-to-space ratio of the gate pattern; and
- uses conventional processes.

Brief Description of the Drawings

The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 is a flowchart of the disclosed process.

Figures 2A-2E show a partially fabricated gate structure, at various steps in the fabrication of the disclosed embodiments.

Detailed Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Presently Preferred Embodiment

A first embodiment of the disclosed process is shown in the flowchart of **Figure 1**, a discussion of which follows in conjunction with Figures 2A-E.

After isolation structures and a gate dielectric **10** (e.g. 5 nm of grown silicon oxide) are formed, a layer of polysilicon **20** is deposited over the dielectric. This is followed by formation of a thin layer of oxide (not shown) and deposition of a layer of nitride **30**, then the layers are patterned to form a gate structure **(step 110)**.

A second layer of nitride is then deposited overall and etched **(step 115)** to form gate sidewall spacers **40**, giving the structure of **Figure 2A**. Note that the original layer of nitride **30** on top of the gate must be thick enough to withstand the overetch necessary to form the spacers. Once the gate is covered with nitride, an oxidation is performed **(step 120)**, which makes the gate oxide **10′** wider under the gate corners than it is near the center of the gate. This is often called a "smiling oxidation", due to the creation of upturned corners in the

oxide; after it is completed, the nitride layer is removed **(step 125)**, giving a structure such as is shown in **Figure 2B**.

Lightly-doped-drain extension regions (LDD regions **70**) are then formed **(step 130)** by implantation of the exposed active area. This is followed by conformal deposition **(step 140)** of a metal **50**, such as 20 nm of titanium, which will be used to form a silicide. This gives the structure shown in **Figure 2C**. After deposition, the source/drain areas receive their final doping, which is implanted **(step 145)** through the layer of metal to form regions **80**. It is noted that the conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant. An additional, optional implant (e.g., high-energy boron for an NMOS device) can be performed at this point **(step 150)**, to form the HALO implant, if desired.

The wafer is then annealed **(step 155)** to form a silicide on the gate and to disperse the dopants. Note that, since the source/drain areas are covered by an oxide, a silicide will not form in these regions. Unreacted metal will be stripped **(step 160)** from the gate area, giving the structure shown in **Figure 2D**. Dielectric spacers can optionally be formed at this point **(step 165)** to protect the gate from accidental contact, and the source/drain areas separately silicided **(step 170)**. It is noted that since the gate and source/drain areas are silicided in separate steps, it is possible to use different metals to form the two silicides.

Processing can then proceed with the usual procedures to complete the wafer.

Alternate Embodiment: Timing of LDD Implant

In an alternate embodiment, the LDD regions are implanted after formation of the nitride sidewalls, but prior to the smiling oxidation. In another alternate embodiment, the LDD regions are implanted prior to the formation of the nitride sidewalls and the source/drain regions are implanted after the nitride sidewalls are formed but before metal deposition.

Alternate Embodiment: Silicon Extensions to Gate

In another alternate embodiment, after the smiling oxidation and nitride removal, a layer of polysilicon or amorphous silicon is deposited and anisotropically etched **(step 135)** to form sidewall extensions **25** of the polysilicon gate, as shown in **Figure 2E**. When this option is used, the thin oxide on top of the gate (not shown) which separates the nitride and the gate is preferably left in place to act as an etch stop for the polysilicon sidewall etch. In the case of amorphous silicon, an anneal step is preferably added to the flow if subsequent steps do not include high enough temperatures to cause the transformation to polysilicon.

Alternate Embodiment: Silicon Germanium.

In another alternative embodiment, the gate structure can consist of a polycrystalline silicon germanium. Other process parameters remain the same.

Alternate Embodiment: Simultaneous Gate and S/D Silicide

In a less preferred embodiment, prior to deposition of metal in step 150, the gate oxide can be removed to allow simultaneous silicidation of the source/drain areas and the gate. In this embodiment, care must be taken to ensure that the gate silicide is not shorted to the source/drain silicides.

Modifications and Variations

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given, but is only defined by the issued claims.

While the inventions have been described with primary reference to a single-poly process, it will be readily recognized that these inventions can also be applied to process with two, three, or more layers of polysilicon or polycide.

The use of the polysilicon sidewall is not necessarily limited to a poly/gate structure. This can be advantageous for future metal/barrier/poly structures, e.g. for W/TiN/silicon structures. It may also be applied to polysilicon-free structures, such as W/TiN/SiO2 structures.

In an alternate embodiment, the disclosed "wide smile" structure, i.e. a gate that has been widened with conductive sidewalls after the "smiling" oxidation, is used without an LDD implant. Instead, a single implant is used, possibly including arsenic as well as phosphorus in the N+ implant, to provide a simpler drain structure.

CLAIMS

What is claimed is:

1. An integrated circuit transistor structure comprising:
a crystalline semiconductor channel region;
a gate dielectric overlying said channel region; and
a conductive gate overlying said gate dielectric, said gate having sidewalls;
wherein said gate dielectric has thicker portions thereof near said sidewalls of said gate than under central portions of said gate;
wherein said thicker portions have a thickness contour corresponding to a lateral oxidation from a starting point which is not aligned with said sidewall of said gate, but is interior to said gate.

2. The integrated circuit transistor structure of Claim 1, wherein said gate comprises a metal silicide.

3. A method for forming a transistor gate structure, comprising the steps of:

(a.) forming a dielectric over a semiconductor region;

(b.) forming a patterned gate over said dielectric;

(c.) performing a lateral growth step which increases the thickness of said dielectric in proximity to sidewalls of said gate, but not under central regions of said gate;

(d.) depositing a metallic material onto sidewalls of said gate;

(e.) reacting said metallic material with said gate to form a conductive compound; and

(f.) stripping unreacted portions of said metallic material;

whereby a gate structure with enhanced conductivity is formed.

4. The method of Claim 3, further comprising the step, between said steps (c.) and (d.), of implanting dopants into said semiconductor region near said gate.

5. The method of Claim 3, further comprising the step, between said steps (d.) and (e.), of implanting dopants into said semiconductor region near said gate.

6. A method for forming a transistor gate structure, comprising the steps of:

(a.) forming a dielectric over a semiconductor region;

(b.) forming a patterned gate over said dielectric;

(c.) performing a lateral growth step which increases the thickness of said dielectric in proximity to sidewalls of said gate, but not under central regions of said gate;

(d.) after said step (c.), forming conductive sidewall spacers on said gate.

7. The method of Claim 6, comprising the additional step, after said step (d.), of forming a dielectric spacer on the sidewalls of said gate, to prevent accidental electrical contact to said gate;

8. A product produced by the method of Claim 3.

9. A product produced by the method of Claim 6.

ABSTRACT

The conductivity of gate structures can be improved by siliciding the entire gate. Additionally, silicon sidewalls can be added to the gate after the "smiling" oxidation, but before silicidation, which provides a new tool for drain profile engineering.

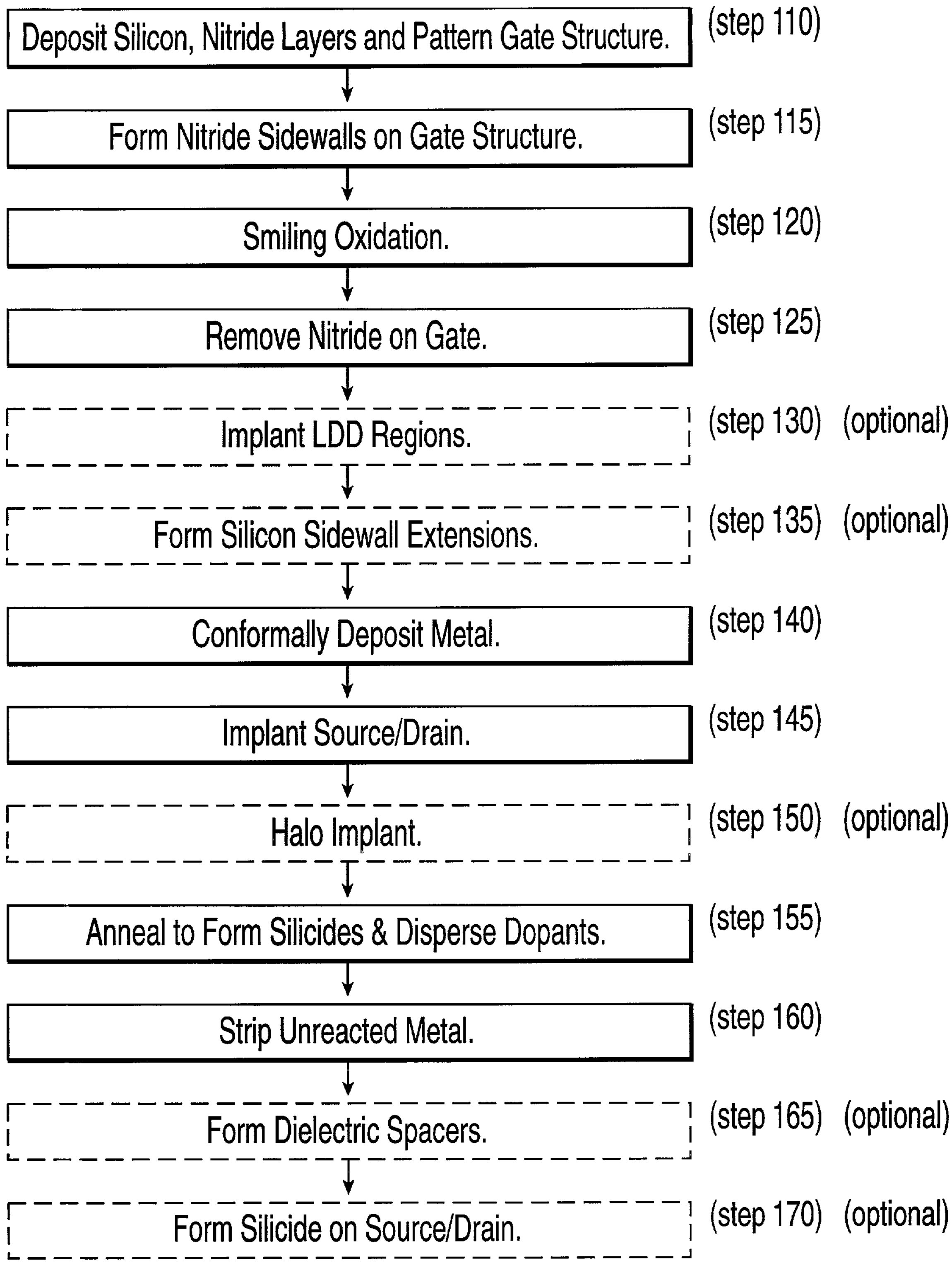
Deposit Silicon, Nitride Layers and Pattern Gate Structure.
(step 110)
Form Nitride Sidewalls on Gate Structure.
(step 115)
Smiling Oxidation.
(step 120)
Remove Nitride on Gate.
(step 125)
Implant LDD Regions.
(step 130) (optional)
Form Silicon Sidewall Extensions.
(step 135) (optional)
Conformally Deposit Metal.
(step 140)
Implant Source/Drain.
(step 145)
Halo Implant.
(step 150) (optional)
Anneal to Form Silicides & Disperse Dopants.
(step 155)
Strip Unreacted Metal.
(step 160)
Form Dielectric Spacers.
(step 165) (optional)
Form Silicide on Source/Drain.
(step 170) (optional)

FIG. 1

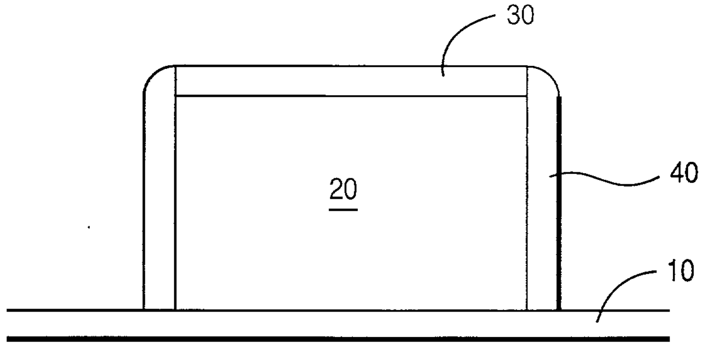

FIG. 2A

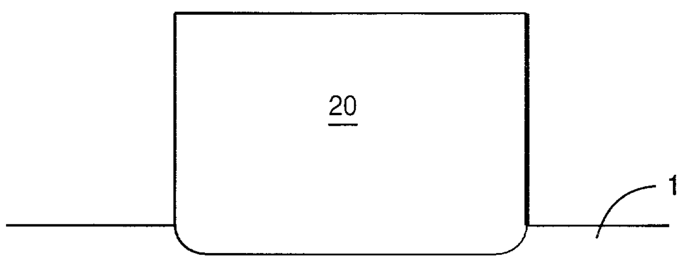

FIG. 2B

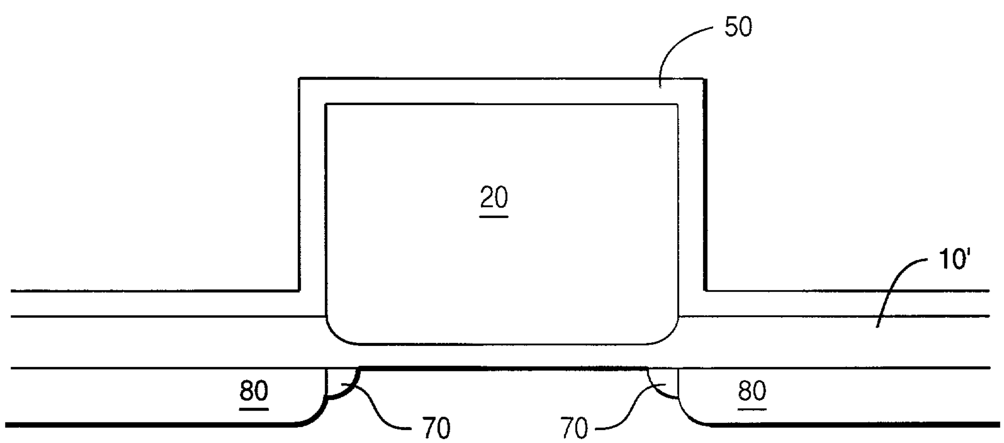

FIG. 2C

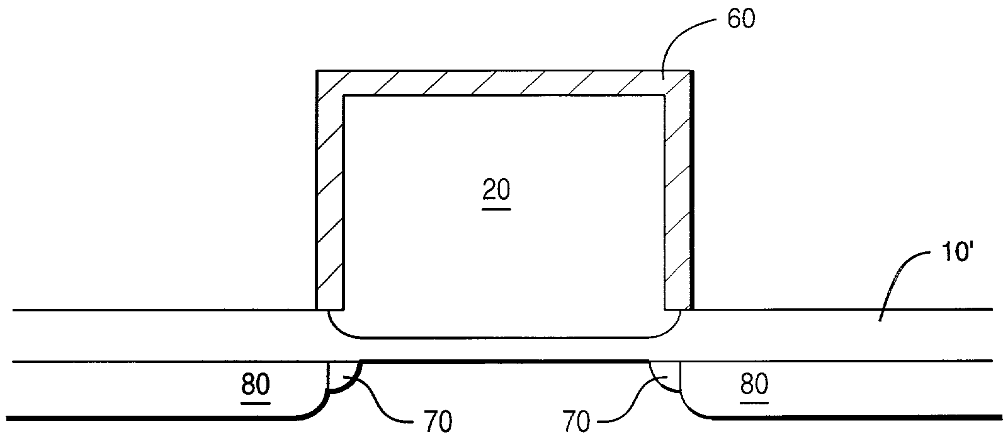

FIG. 2D

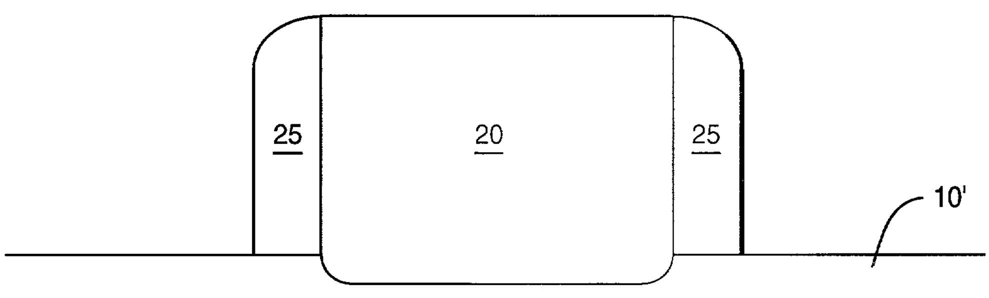

FIG. 2E

ATTORNEY'S DOCKET NO.
T-21570P

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Title of Invention: **Enhancements to Polysilicon Gate;**

Power of Attorney: I hereby appoint the following attorneys to prosecute this application and transact all business in the patent and trademark office connected therewith

Jacqueline J. Garner, Reg. No. 36,144; Wade James Brady III, Reg. No. 32,080;
Mark A. Valetti, Reg. No. 36,707; Carlton H. Hoel, Reg.No. 29,934;
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Inventor: Robert H. Havemann
Date: January 8, 1998 Signature: Robert H. Havemann
Residence and Mailing Address: 7413 Stillwater Court, Garland TX, 75044 Citizenship: U.S.